IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

a first conductivity type well area formed in a surface area of the semiconductor substrate;

a plurality of element isolation areas formed in the well area;

a second conductivity type semiconductor layer formed in a first area of the well area which is isolated by the element isolation areas, the second conductivity type semiconductor layer configuring a first electrode of a capacitor;

a first conductivity type semiconductor layer formed in a second area of the well area which is isolated by the element isolation areas, the first conductivity type semiconductor layer configuring a second electrode of the capacitor; and

a first conductivity type low resistance area ~~which is provided at a base portion of the well area and which connects the first area and the second area, the low resistance area~~ having a resistive value lower than that of the well area, which is in contact with the element isolation areas, and is not in contact with a depletion layer of a junction portion between the second conductivity type semiconductor layer and the well area, and is not in contact with a depletion layer of a junction portion between the first conductivity type semiconductor layer and the well area,

wherein the low resistance area is ~~not in contact with a depletion layer of a junction portion between the second conductivity type semiconductor layer and the well area, and is not in contact with a depletion layer of a junction portion between the first conductivity type~~

~~semiconductor layer and the well area, and is in contact with the element isolation areas~~ in contact with a base portion of the well area and connects said first and second areas.

Claim 2. (Canceled)

Claim 3. (Canceled)

Claim 4. (Original) The device according to claim 1, wherein the low resistance area is situated from the first conductivity type semiconductor layer to the second conductivity type semiconductor layer at a base portion of the well area.

Claim 5. (Original) The device according to claim 1, wherein the impurity concentration of the low resistance area is set to above 2 times that of the well area.

Claim 6. (Original) The device according to claim 5, wherein the impurity concentration of the low resistance area is set to above $1 \times 10^{18}$ $cm^{-3}$.

Claim 7. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

a first well area formed in a surface area of the semiconductor substrate;

a second well area formed in a surface area of the semiconductor substrate;

a plurality of element isolation areas formed in the first and second well areas;

a MOS transistor formed in a first area of the first well which is isolated by the element isolation areas;

a first semiconductor layer with a first conductivity type formed in a second area of the first well area, which is isolated from the MOS transistor by the element isolation areas, the first semiconductor layer being a node for supplying a potential to the first well area; and

a first low resistance area with a first conductivity type ~~which is provided at a base portion of the first well area and which connects the first area and the second area, the first low resistance area~~ having a resistive value lower than that of the first well area, which is in contact with the element isolation areas, and is not in contact with a depletion layer of a junction portion between source/drain regions of the MOS transistor and first well area,

wherein the first low resistance area is ~~not in contact with a depletion layer of a junction portion between source/drain regions of the MOS transistor and first well area, and is in contact with the element isolation areas~~ in contact with a base portion of the first well area and connects said first and second areas.

Claim 8. (Canceled)

Claim 9. (Canceled)

Claim 10. (Previously Presented) The device according to claim 7, wherein the low resistance area is situated from the first conductivity type semiconductor layer to the second conductivity type semiconductor layer at a base portion of the well area.

Claim 11. (Original) The device according to claim 7, wherein the impurity concentration of the low resistance area is set to above 2 times that of the well area.

Claim 12. (Original) The device according to claim 11, wherein the impurity concentration of the low resistance area is set to above $1 \times 10^{18}$ $cm^{-3}$.

Claim 13. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

a first well area with a first conductivity type formed in a surface area of the semiconductor substrate;

a second well area formed in a surface area of the semiconductor substrate;

a plurality of element isolation areas formed in the first and second well areas;

a first electrode with a second conductivity type of a bipolar transistor formed on a first area of the first well area which is isolated by the element isolation areas;

a second electrode with the first conductivity type of the bipolar transistor formed on the first electrode;

a third electrode with the first conductivity type of the bipolar transistor formed in a second area of the first well area which is isolated from the first area by the element isolation area; and

a first low resistance area ~~which is provided at the base portion of the first well area and which connects the first area and the second area, the first low resistance area~~ having a resistive value lower than that of the first well area, which is in contact with the element isolation areas, and is not in contact with a depletion layer of a junction portion of the bipolar transistor,

wherein the first low resistance area is ~~not in contact with a depletion layer of a junction portion of the bipolar transistor and is in contact with the element isolation areas~~ in contact with a base portion of the first well area and connects the first and second areas.

Claim14. (Canceled)

Claim 15. (Canceled)

Claim 16. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate;

a first well area formed in a surface area of the semiconductor substrate;

a second well area formed in a surface area of the semiconductor substrate;

an analog circuit formed in the first well area;

a digital circuit formed in the second well area;

an isolation area formed between the first and second well area; and

a low resistance area provided at a base portion of the first well area excluding the second well area, the low resistance area having a resistive value lower than that of the first well area,

wherein the low resistance area is not in contact with a depletion layer of the analog circuit and in contact with the isolation area.

Claim 17. (Original) The device according to claim 16, wherein the impurity concentration of the low resistance area is set to above 2 times that of the well area.

Claim 18. (Original) The device according to claim 16, wherein the impurity concentration of the low resistance area is set to above $1 \times 10^{18}\,cm^{-3}$.

Claim 19. (Original) The device according to claim 17, wherein the impurity concentration of the first well area where the analog circuit is provided is set to be higher than that of the second well area where the digital circuit is provided.

Claim 20. (Previously Presented) The device according to claim 7, further comprising a second semiconductor layer with a second conductivity type formed at a third area of the second well area which is isolated by the element isolation areas, the second semiconductor layer configuring a first electrode of a capacitor;

a third semiconductor layer with the first conductivity type formed in a fourth area of the second well area which is isolated by the element isolation areas, the third semiconductor layer configuring a second electrode of the capacitor; and

a second low resistance area with the first conductivity type which is provided at a base portion of the second well area and which connects the third area and the fourth area, the second low resistance area having a resistive value lower than that of the second well area,

wherein the second low resistance area is not in contact with a depletion layer of a junction portion between the second semiconductor layer and the second well area, and is not in contact with a depletion layer of a junction portion between the third semiconductor layer and the second well area, and is in contact with the element isolation areas.

Claim 21. (Previously Presented) The device according to claim 20, further comprising a wiring layer connected to the second semiconductor layer and one of source/drain regions of the MOS transistor.

Claim 22. (Previously Presented) The device according to claim 1, wherein the capacitor is a variable capacitance capacitor.

Claim 23. (Previously Presented) The device according to claim 20, wherein the capacitor is a variable capacitance capacitor.

Claim 24. (Previously Presented) The device according to claim 13, further comprising a second semiconductor layer with a second conductivity type formed at a third area of the second well area which is isolated by the element isolation areas, the second semiconductor layer configuring a first electrode of a capacitor;

a third semiconductor layer with the first conductivity type formed in a fourth area of the second well area which is isolated by the element isolation areas, the third semiconductor layer configuring a second electrode of the capacitor; and

a second low resistance area with the first conductivity type which is provided at a base portion of the second well area and which connects the third area and the fourth area, the second low resistance area having a resistive value lower than that of the second well area,

wherein the second low resistance area is not in contact with a depletion layer of a junction portion between the second semiconductor layer and the second well area, and is not in contact with a depletion layer of a junction portion between the third semiconductor layer and the second well area, and is in contact with the element isolation areas.

Claim 25. (Previously Presented) The device according to claim 24, wherein the capacitor is a variable capacitance capacitor.

Claim 26. (Previously Presented) The device according to claim 1, wherein a bottom portion of the low resistance area is lower than that of the element isolation area.

Claim 27. (Previously Presented) The device according to claim 7, wherein a bottom portion of the low resistance area is lower than that of the element isolation area.

Claim 28. (Previously Presented) The device according to claim 13, wherein a bottom portion of the low resistance area is lower than that of the element isolation area.